

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

	States Patent and Fragemark Office
Address:	COMMISSIONER FOR PATENTS
	P.O. Box 1450
	Alexandria, Virginia 22313-1450
	MANAN TIRUTU GUA

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/648,271	08/25/2000	Petro Estakhri	LEXA-00301	5878	
28960	7590 02/11/2004		EXAM	INER	
HAVERSTOCK & OWENS LLP			TRAN, DENISE		
	WOLFE ROAD E, CA 94086		ART UNIT	PAPER NUMBER	
			2186	N/	
			DATE MAILED: 02/11/200	4	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicati	on No.	Applicant(s)			
		09/648,2	71	ESTAKHRI ET AL.			
	Office Action Summary	Examine	r	Art Unit			
		Denise	Tran	2186			
Period fo	The MAILING DATE of this communication	n appears on th	e cover sheet with the	correspondence address			
A SH THE - Exte after - If the - If NO - Failu - Any	IORTENED STATUTORY PERIOD FOR R MAILING DATE OF THIS COMMUNICATION IN SIGN (6) MONTHS from the mailing date of this communication ED (7) ED (8) MONTHS from the mailing date of this communication ED period for reply specified above, the maximum statutory pure to reply within the set or extended period for reply will, by reply received by the Office later than three months after the ed patent term adjustment. See 37 CFR 1.704(b).	ON. FR 1.136(a). In no exon. , a reply within the state oriod will apply and vistatute, cause the approximation.	vent, however, may a reply be ti tutory minimum of thirty (30) da rill expire SIX (6) MONTHS from plication to become ABANDON	mely filed ys will be considered timely. n the mailing date of this communication. ED (35 U.S.C. § 133).			
1)⊠	Responsive to communication(s) filed on	<u>09 January 200</u>	<u>04</u> .				
2a) <u></u> ☐	This action is FINAL . 2b)	This action is n	on-final.				
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposit	ion of Claims						
4)⊠	☑ Claim(s) <u>1-66</u> is/are pending in the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5)⊠	Claim(s) <u>1-13 and 27-49</u> is/are allowed.						
6)⊠	Claim(s) 14,19,20,25,26,50-54 and 60-66 is/are rejected.						
7)⊠	Claim(s) <u>15-18,21-24 and 55-59</u> is/are obj	jected to.					
8)[Claim(s) are subject to restriction a	and/or election i	equirement.				
Applicat	ion Papers						
9)🛛	The specification is objected to by the Exa	miner.					
10)🖾	The drawing(s) filed on 25 August 2000 is/	/are: a)□ acce	epted or b)⊠ objected	to by the Examiner.			
	Applicant may not request that any objection to	o the drawing(s)	be held in abeyance. Se	ee 37 CFR 1.85(a).			
	Replacement drawing sheet(s) including the co	orrection is requi	red if the drawing(s) is ol	pjected to. See 37 CFR 1.121(d).			
11)	The oath or declaration is objected to by the	ne Examiner. N	ote the attached Office	e Action or form PTO-152.			
Priority (under 35 U.S.C. §§ 119 and 120			·			
* (13)	Acknowledgment is made of a claim for for All b) Some * c) None of: 1. Certified copies of the priority docur 2. Certified copies of the priority docur 3. Copies of the certified copies of the application from the International But See the attached detailed Office action for a Acknowledgment is made of a claim for doraince a specific reference was included in the Acknowledgment is made of a claim for doraince as a pecific reference was included in the Acknowledgment is made of a claim for doraince compared to the foreign language and the Acknowledgment is made of a claim for doraince was included in the first sentence	ments have been ments have been priority docum ureau (PCT Ru a list of the cert mestic priority une first sentence provisional apmestic priority unestic priority unestication priority un	en received. en received in Applicatents have been received le 17.2(a)). ified copies not receivender 35 U.S.C. § 1190 of the specification of the specification of the specification of the 35 U.S.C. §§ 120 of the Specification has been respecification than the specification has been respectively.	tion No red in this National Stage ed. (e) (to a provisional application) or in an Application Data Sheet. ceived. 0 and/or 121 since a specific			
Attachmer			A) [] (mt	(OTO 442) Depart No(a)			
2) 🔲 Notic	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-94) mation Disclosure Statement(s) (PTO-1449) Paper N			y (PTO-413) Paper No(s) Patent Application (PTO-152)			

Application/Control Number: 09/648,271 Page 2

Art Unit: 2186

DETAILED ACTION

1. Claims 1-66 are presented for examination.

- 2. Figures 1, 3, and 5-6 should be designated by a legend such as --Prior Art--because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
- 3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of **50 to 150 words**. Correction is required. See MPEP § 608.01(b).

Application/Control Number: 09/648,271 Page 3

Art Unit: 2186

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The current specification, e.g., page 13, lines 25-30 fails to provide proper antecedent basis for the claimed feature claim 50, lines 6-7, "... Dedicated Overhead Blocks for storing Overhead Data including a first Dedicated Data Block and a second Dedicated Data Block".

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 14, 19-20, 25, 50-54, 60-63 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by lida et al., U.S. Patent No. 6,625,713 B2 (hereinafter lida).

As per claim 50, lida teaches a flash memory device for storing user data comprising a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses (i.e., segments or blocks, e.g., cols 5-6, figs. 7, 11 and 14) including:

Art Unit: 2186

a plurality of dedicated data blocks for storing user data (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks n-1 and n; col. 5, line 55 to col. 6, line 20); and

a plurality of dedicated overhead blocks for storing overhead data including a first dedicated data block and a second dedicated data block (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20).

As per claim 14, lida teaches a method of data storage within a flash memory comprising the steps:

Mapping a non volatile memory medium within the flash memory system into a plurality of independently addressable, independently programmable and independently erasable blocks (i.e., segments or blocks, e.g., cols 5-6, figs. 7, 11 and 14) including a plurality of dedicated data blocks (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks n-1 and n; col. 5, line 55 to col. 6, line 20) and a plurality of dedicated overhead blocks comprising a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20; fig. 14C segments or block 123);

Mapping each of the plurality of dedicated overhead blocks into a plurality of consecutive address overhead segments (e.g., figs. 14b-c, pages 0-15) wherein the plurality of segments within each dedicated overhead block are address according to an

Application/Control Number: 09/648,271

Art Unit: 2186

identical set of distinct segment addresses (e.g., figs. 14b-c, pages 0-15), each segment comprising: physical address register for storing a physical address for locating corresponding user data (e.g., fig. 14 D, 003; col. 12, lines 16-18); and a flag field (e.g., figs.14 B-C, control flag); and

correlating first group of virtual logical block addresses including a first VLBA to the first dedicated overhead block (e.g., figs 14, redundant portion, logical address).

As per claims 51-54, lida teaches, wherein each dedicated overhead block is identically comprised of a plurality of separately addressable overhead pages, each block following an identical sequence of page addresses (i.e., blocks or pages; e.g., fig. 7A, blocks 1-3; or fig. 7D, pages 0-m); wherein each overhead page is comprised of a plurality of independently addressable and independently programmable segments (i.e., pages; e.g., fig. 7D, pages 0-m); wherein the plurality of independent overhead segments are used for storing overhead data, each overhead segment supporting one virtual logical block of user data (e.g., figs. 7E-F, redundant portion, logical address), each overhead segment comprising: physical address register for storing a physical address for locating corresponding user data (e.g., fig. 14 D, 003; col. 12, lines 16-18); and a flag field (e.g., figs.14 B-C, control flag); and lida shows wherein a first group of virtual logical block addresses including a first VLBA are assigned to the first dedicated overhead block, such that overhead data generated in support of the first VLBA will be stored in an overhead segment within the first dedicated overhead block (e.g., figs 14, redundant portion, logical address).

Art Unit: 2186

As per claims 19-20, 25, 60-63 and 65, lida shows a controller for regulating and controlling the operation of the flash memory (e.g., fig. 4, el. 109); a volatile ram space manager comprising a plurality of correlation fields for correlating virtual addresses and physical addresses or storing a logical address within a non-volatile correlation register within the flash memory system (e.g., fig. 4, el. 111; and col. 13, lines 15-25 and col. 20, lines 30-35); the space manager comprises a flag register comprising a plurality of status flags (e.g., fig. 7F, status flags; fig. 14D, control table flags); a means for loading data from a non volatile memory area into a correlation register of the RAM space manager on start up or power up (e.g., col. 20, lines 30-35); means for generating error correction data corresponding to user (e.g., col. 7, lines 1-30

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over lida et al., U.S. Patent No. 6,625,713 B2 (hereinafter lida) as applied to claim 50 above, and further in view of applicant's admitted prior art, the current specification pages 2-12 and figs. 1-6 (hereinafter AAPA).

As per claim 64, lida shows a means for loading data from a nonvolatile memory area into the space manager on start up (e.g., col. 20, lines 30-35). Iida does not

Application/Control Number: 09/648,271

Art Unit: 2186

explicitly shows the use of a reset command. AAPA shows the use of a reset command (e.g., page 11, lines 20-26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of AAPA into the system of lida because it would allow the system to recover data from the system failure.

10. Claims 26 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over lida et al., U.S. Patent No. 6,625,713 B2 (hereinafter lida) as applied to claims 50 or 14 above, and further in view of Tanaka, U.S. Patent No. 6,446177 B1 (hereinafter Tanaka).

As per claims 26 and 66, lida shows a dedicated data block to function as a dedicated overhead block and an existing dedicated overhead block (e.g., col. 11, line 65- col. 12, line 15). Iida does not explicitly shows means for re-designating a block in the even of failure of an existing block. Tanaka shows means for re-designating a block in the even of failure of an existing block (e.g., page 28, lines 40-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Tanaka into the system of lida because it would allow the system to recover data from the defective block.

11. Claims 1-13 and 27-49 are allowed.

Page 7

- 12. Claims 15-18, 21-24, and 55-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- a) Kimura et al. (6282624) show an address conversion table stored in a nonvolatile memory for improved access at power up.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for

Application/Control Number: 09/648,271

Art Unit: 2186

Page 9

the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

D.T.

Febuary, 6, 2004